Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	(treating with substrate) same (high adj density adj plasma)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:12
L2	15	1 and (Si or silicon or Zn or zinc)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:12
L3	14	2 and oxide	US-PGPUB; USPAT	OR	ON	2005/07/13 12:54
L4	18	(treating with substrate) same (high adj density adj plasma)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/13 13:54
L5	275	(treating with substrate) and (high adj density adj plasma)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:12
L6	94	5 and (forming with oxide)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:12
L7	84	6 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/13 13:55
L8	82	7 not 2	US-PGPUB; USPAT	OR	ON	2005/07/13 15:09
L10	1465	(treating with substrate) same plasma	US-PGPUB; USPAT	OR	ON	2005/07/13 13:54
L11	163	10 and ((high adj density) with plasma)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:55
L12	148	11 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/13 13:55
L13	128	12 not 7	US-PGPUB; USPAT	OR	ON	2005/07/13 13:55
L14	117	13 not 2	US-PGPUB; USPAT	OR	ON	2005/07/13 13:55
L15	20	14 and (forming same oxide)	US-PGPUB; USPAT	OR	ON	2005/07/13 13:56
L16	26	(treating with plasma) same ICP	US-PGPUB; USPAT	OR	ON	2005/07/13 15:47
L17	24	16 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/13 15:48
L18	20	17 and temperature	US-PGPUB; USPAT	OR	ON	2005/07/13 15:10
L19	77	(treating with plasma) same (ECR or (cathode adj coupled))	US-PGPUB; USPAT	OR	ON	2005/07/13 16:02
L20	76	19 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/13 16:04
L21	57	20 and oxide	US-PGPUB; USPAT	OR	ON	2005/07/13 15:48
L22	0	(treating with plasma) same (transmission adj coupled)	US-PGPUB; USPAT	OR	ON	2005/07/13 16:02

L23	2	(treating with plasma) same (transmission with coupled)	US-PGPUB; USPAT	OR	ON	2005/07/13 16:03
L24	1	(treating with plasma) same (transformer with coupled)	US-PGPUB; USPAT	OR	ON	2005/07/13 16:04
L25	35	plasma and (transformer with transmission with coupled)	US-PGPUB; USPAT	OR	ON	2005/07/13 16:04
L26	27	25 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/13 16:04

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8650	(ECR or (cathode adj coupled adj plasma))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:10
L2	408	1 and (treating with (substrate or silicon))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:05
L3	111	1 and (oxide same (treating with (substrate or silicon)))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:05
L4	109	(treating same (ECR or (cathode adj coupled adj plasma)))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:05
L5	66	4 and (treating with (substrate or silicon))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:05
L6	18	5 and (oxide same (treating with (substrate or silicon)))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:10
L7	1118	(high adj density adj plasma) same (ECR or (cathode adj coupled adj plasma))	US-PGPUB; USPAT	OR	ON	2005/07/23 10:10
L8	815	7 and (oxide same silicon)	US-PGPUB; USPAT	OR	ON	2005/07/23 10:11
L9	583	7 and (plasma same oxide same silicon)	US-PGPUB; USPAT	OR	ON	2005/07/23 10:11
L10	554	9 and @ad<"20040315"	US-PGPUB; USPAT	OR	ON	2005/07/23 10:11

DOCUMENT-IDENTIFIER: US 20040233608 A1

TITLE: Apparatus and methods for compensating plasma sheath non-uniformities at the substrate in a plasma processing system

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (5):

[0003] The uniformity of the plasma processing of the substrate's exposed surface is a function of the uniformity of ion flux and ion energy, among other variables. The electrostatic chuck in inductively-coupled plasma (ICP) source systems may be biased independently with radio-frequency power so that the ion energy at the substrate can be varied without varying the ion flux at the substrate. The uniformity of the ion flux at the substrate is primarily determined by the plasma density distribution. Plasma density distributions in a plasma processing system equipped with an ICP source exhibit a prominent central peak near the azimuthal centerline of the chamber and decrease radially from the central peak toward the sidewall, which is typically cylindrical. FIG. 1 shows the radial dependence of the electron density and plasma **temperature** in a prior art ICP processing system. Therefore, the uniformity of the plasma processing is reduced by the radial dependence of the plasma density distribution, which is of particular concern for large diameter substrates.

Brief Description of Drawings Paragraph - DRTX (3):

[0014] FIG. 1 is a graphical representation of the plasma density, the electron **temperature,** the plasma sheath capacitance, and the sum of the plasma sheath capacitance and wafer capacitance for a portion of a plasma proximate to the substrate-supporting surface of an electrostatic chuck in a plasma processing system in accordance with the prior art;

Detail Description Paragraph - DETX (2):

[0037] With reference to FIG. 2, a **plasma** processing system 10 operable for **treating** a substrate 12, such as a semiconductor wafer, with an inductively-coupled **plasma (ICP)** is depicted. Processing system 10 includes a processing chamber 14 that encloses a processing space 16 with a grounded sidewall. The processing system 10 is provided with a plasma power source 18 electrically connected in a known manner to an antenna 20 positioned adjacent to a planar dielectric window 22, which forms a sealed portion of the

processing chamber 14. The plasma power source 18 conventionally includes a radio-frequency (RF) power supply and appropriate RF matching circuitry adapted for efficient coupling of RF power, typically at 13.56 MHz, to the antenna 20. Antenna 20 directs RF power through the dielectric window 22 into the processing space 16 for generating and sustaining a plasma 24 in processing space 16 by interacting with a rarified atmosphere of a partial pressure of process gas, such as argon, provided in processing chamber 14. Typically, the plasma power source 18 operates at a frequency of between about 440 kHz and about 13.56 MHz and outputs an RF power of up to about 5000 watts. Collectively, the plasma power source 18, antenna 20 and dielectric window 22 define a plasma generator operative to generate plasma 24 in processing space 16, which is used for processing an exposed surface of substrate 12.

Detail Description Paragraph - DETX (5):

[0040] With continued reference to FIG. 2, an electrostatic chuck (ESC) 30 is mounted within the processing chamber 14 opposite to the antenna 20. The electrostatic chuck 30 is used to heat or cool the substrate 12, electrically bias the substrate 12, and support the substrate 12 in a stationary state proximate the plasma 24 in the vacuum processing space 16. The electrostatic chuck 30 includes a metal body 32 covered by a planarization dielectric coating 34. The planarization dielectric coating 34 has a substrate-supporting surface 36 that faces the plasma 24 and upon which the substrate 12 is positioned. Electrodes 38, 40 embedded in the planarization dielectric coating 34 are biased with a DC clamping voltage supplied by a variable, high-voltage power supply 39. An RF power supply 41 is electrically coupled with the electrodes 38, 40 for providing a time-dependent DC bias that attracts ions and radicals from the plasma 24 to the exposed surface of the substrate 12. Electrostatic chuck 30 incorporates other conventional structures as understood by persons of ordinary skill in the art, such as heating elements, **temperature** sensors, and passageways for heat transfer gas.

Detail Description Paragraph - DETX (6):

[0041] When plasma 24 is present in the processing chamber 14, the electron density (n.sub.e) and the electron **temperature** (T.sub.e) are functions of the spatial location within plasma 24 and functions of plasma conditions, such are gas pressure (p.sub.Ar), input RF power (P.sub.RF), electrode geometry, and coil geometry. Formally, this dependence can be expressed as:

Detail Description Paragraph - DETX (18):

[0048] In low pressure plasmas generated with an ICP plasma source, the electron **temperature** is relatively small, around 1-2 eV, and biases up to about -100 VDC, such that the plasma sheath thickness is about

d.sub.s.congruent.32.lambda..sub.D.

Detail Description Paragraph - DETX (21):

[0051] The sheath capacitance may be expressed as a function of the plasma parameters, electron density and the electron **temperature**. Due to radial non-uniformities in the electron density and electron **temperature,** the capacitance of the plasma sheath 42 at the substrate-supporting surface 36 facing the plasma 24 will be radially non-uniform. The capacitance of the plasma sheath 42 per unit area at the substrate-supporting surface 36 of the electrostatic chuck 30, after substituting for d.sub.S, is expressed as: 5 C sheath ESC = 1.224 .times. 10 - 3 r 0 n e 1 / 2 T e 1 / 4 (V p - V B) 3 / 4

Detail Description Paragraph - DETX (22):

[0052] where electron density (n.sub.e) is in cm.sup.-3, electron **temperature** (T.sub.e) is in eV, and potentials (V.sub.B) and (V.sub.P) are in volts, and (.di-elect cons..sub.r) is the dielectric constant of a vacuum. Similarly, on the grounded sidewall of processing chamber 14, the specific capacitance of the plasma sheath 42 can be expressed as: 6 C sheath wall = C sheath wall (n e , T e) , e . g . C sheath wall = 1.224 .times. 10 - 3 r 0 n e 1 / 2 T e 1 / 4 V p 3 / 4

Detail Description Paragraph - DETX (24):

[0054] The sheath capacitance possesses radial inhomogeneities or non-uniformities manifested by radial non-uniformities in plasma parameters, such as electron density, electron **temperature,** or plasma potential, or by radial non-uniformities in process parameters such as etch rate, deposition rate, and film thickness. Plasma properties are measured proximate to the substrate-supporting surface 36 of the electrostatic chuck 30 and process properties are evaluated by examining the processed wafer. The design process will be described below in relation to FIG. 15.

Detail Description Paragraph - DETX (33):

[0063] With reference to FIG. 4, the total specific capacitance of the dielectric material the planarization dielectric coating 34 filling and overlying the one-dimensional linear grid of grooves 52 and ridges 56 (FIGS. 3, 3A) is graphically illustrated as a function of the parameters .alpha. and .beta., in which alumina (.di-elect cons..sub.r=9.5) is chosen as the dielectric material constituting the planarization dielectric coating 34 and the maximal thickness of the planarization dielectric coating 34 is 1 mm. Generally, the total specific capacitance increases with increasing .alpha. for constant .beta., which denotes that the total specific capacitance increases as the grooves 52 narrow. Generally, the total specific capacitance

decreases with increasing .beta. for constant .alpha., which denotes that the total specific capacitance decreases as the difference between the minimal and maximal lessens. The total specific capacitance may be displayed graphically, as in FIG. 4, for other dielectric materials having a different dielectric constant, such as quartz (.di-elect cons..sub.r=3.8), in which case the family of curves will shift vertically. Electrostatic chucks may be designed with one-dimensional linear grids (FIG. 3) selected using FIG. 4 as a guideline in order to compensate for observed radial inhomogeneities or non-uniformities in plasma parameters, such as electron density, electron **temperature,** or plasma potential, or process parameters such as etch rate, deposition rate, and film thickness.

Detail Description Paragraph - DETX (58):

[0088] With reference to FIG. 15, a process is described for adjusting a parameter related to plasma conditions at the substrate-supporting surface of an electrostatic chuck in order to correct a process non-uniformity relating to a parameter .xi..sub.i=.xi..sub.i(r) relating to plasma conditions. The process non-uniformity may be characterized by a radial dependence of a plasma parameter, such as plasma density, electron **temperature,** and plasma potential, or by a radial dependence of another process parameter, including but not limited to etching rate, deposition rate, and film thickness, that is directly correlated with plasma parameters. In block 150, the process non-uniformity may be estimated by direct measurement of the plasma parameters near the exposed surface of the electrostatic chuck or by measurement of the process parameter, such as etch or deposition rate, from the processed substrate.

Claims Text - CLTX (22):

21. The method of claim 20 wherein the plasma-related parameter is selected from the group consisting of plasma density, electron **temperature,** and plasma potential.

DOCUMENT-IDENTIFIER: US 20040152342 A1

TITLE: Method of eliminating residual carbon from flowable oxide fill

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

Methods of **forming an oxide** layer such as high aspect ratio trench isolations, and **treating the oxide substrate** to remove carbon, structures formed by the method, and devices and systems incorporating the **oxide** material are provided.

Summary of Invention Paragraph - BSTX (2):

[0001] The invention relates generally to semiconductor processing methods of **forming** and utilizing insulative materials for electrical isolation in integrated circuits, and more particularly to a post-deposition treatment of flowable **oxide** fill materials to eliminate residual carbon from the material.

Summary of Invention Paragraph - BSTX (11):

[0008] In one aspect, the invention provides a method of **treating** a carbon-containing oxide layer disposed on a semiconductive **substrate,** for example, in a trench or other opening in the **substrate,** by exposing the oxide layer to an oxygen plasma to eliminate a substantial amount of carbon from the oxide layer. The oxygen plasma can be formed in the reaction chamber or remotely in a downstream plasma system and then flowed into the chamber. The post-deposition oxygen plasma treatment preferably reduces the carbon in the oxide layer to a non-detectable level, and preferably to about 5% or less.

Summary of Invention Paragraph - BSTX (12):

[0009] In another aspect, the post-deposition oxygen plasma treatment can be used in a method of **forming an oxide** layer on a semiconductor substrate. In one embodiment, the method comprises depositing a layer of a carbon-containing flowable oxide on the substrate by chemical vapor deposition of an organosilane (e.g., trimethylsilane) and an oxygen source gas (e.g., ozone), and conducting an oxygen plasma treatment according to the invention to reduce or eliminate carbon from the oxide layer, preferably to a non-detectable level. The flowable oxide material can be deposited to substantially fill high aspect ratio gaps or openings (e.g., a trench) without leaving voids, and the oxygen plasma treatment is then conducted to reduce the carbon content of the fill

material to a desired level, preferably to about 5% or less.

Summary of Invention Paragraph - BSTX (13):

[0010] In another embodiment, the method comprises **forming** a flowable **oxide** on a substrate, for example, by spin-coating or flow coating, and then exposing the carbon-containing **oxide** material to an oxygen plasma in accordance with the invention to drive out a substantial amount of the carbon from the **oxide** layer.

Summary of Invention Paragraph - BSTX (14):

[0011] In yet another embodiment, the method of the invention comprises depositing an oxide material into a high aspect ratio opening such as a deep trench with a flowable oxide material to partially fill the opening (e.g., about one-half of the depth), and then depositing oxide material by **high density plasma** chemical vapor deposition (HDPCVD) to fill the rest of the opening. This method advantageously eliminates the formation of voids in the fill that can occur when solely a **high density plasma** oxide is used to fill a high aspect ratio gap.

Summary of Invention Paragraph - BSTX (15):

[0012] In another aspect, the invention provides an oxide fill disposed on a semiconductor substrate, which comprises a flowable oxide material treated with an oxygen plasma such that carbon in the oxide material is substantially reduced, preferably to a non-detectable level. Preferably, the oxygen plasma-treated oxide material contains substantially no voids and has a carbon content of about 5% or less. The oxide fill can be disposed, for example, within a high aspect ratio opening such as a deep trench in a semiconductor substrate. The oxide fill material can be formed on the substrate as a flowable oxide by chemical vapor deposition of an organosilane (e.g., trimethylsilane) and an oxygen source gas (e.g., ozone), or, in another embodiment, by a liquid application process such as a spin-on technique of a flowable oxide material. In another embodiment, the oxygen plasma-treated oxide fill can comprise a portion of a flowable oxide material and another portion of **high density plasma** oxide.

Brief Description of Drawings Paragraph - DRTX (4):

[0018] FIG. 5-7 are diagrammatic cross-sectional views of a fragment of a semiconductor wafer substrate at sequential processing steps showing fabrication of a trench isolation according to another embodiment of the method of the invention. FIG. 5 shows formation of a flowable oxide layer in a portion of the trench. FIG. 6 depicts formation of an overlying **high density plasma** oxide layer. FIG. 7 depicts an oxygen plasma treatment of the oxide

fill within the trench.

Detail Description Paragraph - DETX (4):

[0022] The invention provides methods for **forming** a void-free flowable **oxide** layer in a semiconductor substrate and substantially eliminating carbon from the fill material.

Detail Description Paragraph - DETX (10):

[0028] In one embodiment according to the invention, the trenches 14 are filled by reacting TMS with O.sub.3 in vapor form within a CVD reaction chamber. In the reaction chamber, the wafer is heated and a chemical reaction of the precursor gases occurs. Typical deposition process parameters include a chamber pressure maintained at about 50 to about 500 torr, preferably about 300 torr, and a substrate temperature of up to about 800.degree. C., preferably about 20 to about 450.degree. C., preferably about 50 to about 200.degree. C., and more preferably at about 125.degree. C. TMS and O.sub.3, and optionally a carrier gas (e.g., argon, helium, etc.), are flowed into the reaction chamber, and the TMS and O.sub.3 react and gases condense onto the bottom surfaces 16 of the trenches to form a layer of flowable silicon dioxide material, such as layer 20 shown in FIG. 2, incorporating carbon in the form of methyl groups (CH.sub.3). The flowable **oxide** material fills the trenches from the bottom surface up to the top of the trench, thereby avoiding **forming** voids in the center of the fill.

Detail Description Paragraph - DETX (23):

[0041] FIGS. 5-7 illustrate steps in another embodiment of a method in accordance with the invention for **forming an oxide** fill in an opening in a substrate of a wafer fragment 10'. Referring to FIG. 5, a portion (e.g., about one-half) of a trench 14' disposed in a substrate 12' is filled with an oxide layer 20' comprising a flowable oxide material, as described hereinabove. The remainder of the opening 14' can then be filled with a **high density plasma** oxide material 24' using a conventional **high density plasma** chemical vapor deposition (HDPCVD). Briefly, the silicon oxide is deposited in a reaction zone of a HDPCVD reactor while providing a selected bias power, source power and gas mixtures. Exemplary silicon source gases include, for example, silicon tetrachloride (SiCl.sub.4), silicon tetrabromide (SiBr.sub.4), dichlorosilane (SiH.sub.2Cl.sub.2), and disilane (Si.sub.2H.sub.6). Exemplary gases to react with the silicon source gas include oxygen, ozone, nitrous oxide (N.sub.2O), and nitric oxide (NO), for example, along with a carrier gas such as argon or helium.

Claims Text - CLTX (2):

1. A method of **treating** a carbon-containing oxide layer disposed on a semiconductive **substrate,** comprising the step of: exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (6):

5. A method of **treating** a carbon-containing oxide layer disposed on a semiconductive **substrate,** comprising the step of: exposing the oxide layer to an oxygen plasma to reduce the carbon in the oxide layer by at least about 80%.

Claims Text - CLTX (7):

6. A method of **treating** a carbon-containing oxide layer disposed on a semiconductive **substrate,** comprising the step of: exposing the oxide layer to an oxygen plasma for at least about 10 seconds at a **substrate** temperature of up to about 800.degree. C.

Claims Text - CLTX (10):

9. A method of **treating** a carbon-containing oxide layer in a semiconductive **substrate,** comprising the step of: exposing the oxide layer to an oxygen plasma for a time effective to reduce carbon in the oxide layer to a non-detectable level.

Claims Text - CLTX (14):

13. A method of **treating** a carbon-containing oxide layer disposed on a semiconductive **substrate,** comprising the step of: depositing the oxide layer as a flowable oxide to fill a gap within the **substrate**; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (15):

14. A method of **treating** an oxide layer disposed on a semiconductive **substrate,** comprising the steps of: depositing an organosilane and an oxygen source gas by chemical vapor deposition onto the **substrate** to form a carbon-containing flowable oxide layer; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (16):

15. A method of **treating** an oxide layer disposed on a semiconductive **substrate,** comprising the steps of: depositing trimethylsilane and ozone by chemical vapor deposition to form a carbon-containing flowable oxide layer within a gap in the **substrate**; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (17):
16. A method of **treating a substrate,** comprising the step of: heating the **substrate** comprising a carbon-containing flowable oxide layer in a reaction chamber to a temperature of up to about 800.degree. C.; maintaining a pressure within the reaction chamber at about 0.1 to about 20 torr; and exposing the substrate to an oxygen plasma for a time effective to eliminate a substantial amount of carbon from the oxide layer.

Claims Text - CLTX (21):
20. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (35):
34. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (42):
41. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate by chemical vapor deposition of trimethylsilane and ozone; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (43):
42. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate; heating the substrate to a temperature of up to about 20-450.degree. C.; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (44):
43. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon to fill a gap in the substrate; and exposing the oxide layer to an oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (46):
45. A method of **forming an oxide** layer on a semiconductor substrate,

comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate; forming an oxygen plasma in a downstream plasma system; flowing the oxygen plasma into the reaction chamber; and exposing the oxide layer to the oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (47):

46. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: depositing a layer of flowable **oxide** comprising carbon on the substrate; forming an oxygen plasma in the reaction chamber; and exposing the oxide layer to the oxygen plasma to substantially eliminate carbon from the oxide layer.

Claims Text - CLTX (48):

47. A method of **forming an oxide** layer on a semiconductor substrate, comprising the steps of: spin applying a layer of flowable **oxide** comprising carbon to fill a gap within the substrate disposed in a reaction chamber; providing an oxygen plasma in the reaction chamber; and exposing the oxide layer to the oxygen plasma to reduce the carbon content of the oxide layer to a non-detectable level.

Claims Text - CLTX (62):

61. A method of filling an opening in a substrate, comprising the steps of: depositing a layer of flowable oxide comprising carbon to partially fill the opening; depositing a layer of **high density plasma** oxide to fill the opening; and exposing the oxide layer to an oxygen plasma to reduce the carbon in the oxide layer by at least about 80%.

Claims Text - CLTX (74):

73. An oxide fill disposed within an opening in a semiconductor substrate, and comprising an oxygen plasma treated flowable oxide material having substantially no voids and a carbon content of less than about 10%, the fill comprising a layer of a flowable oxide and an overlying layer of a **high density plasma** oxide.

Claims Text - CLTX (96):

95. An electronic system, comprising: a processor; and an integrated circuit in communication with the processor, the integrated circuit comprising a substrate and an oxide fill disposed in an opening in the substrate, the oxide fill comprising an oxygen plasma treated flowable oxide having a carbon content of less than about 10%, the fill comprising a layer of a flowable oxide and an overlying layer of a **high density plasma** oxide.

US-PAT-NO: 6716740

DOCUMENT-IDENTIFIER: US 6716740 B2

TITLE: Method for depositing silicon oxide incorporating an outgassing step

---------- KWIC ---------

Brief Summary Text - BSTX (2):

The present invention generally relates to a method for depositing an inter-metal-dielectric (IMD) layer on a semiconductor **substrate** and more particularly, relates to a method for depositing a silicon oxide dielectric layer on a silicon wafer by plasma enhanced chemical vapor deposition incorporating a heat-**treating** step for outgassing prior to the deposition process.

Detailed Description Text - DETX (2):

The present invention discloses a method for depositing an inter-metal-dielectric layer on a semiconductor **substrate** by plasma chemical vapor deposition incorporating the additional step of heat-**treating** for outgassing impurity gases from the wafer surface prior to the deposition step such that cracking of the IMD layer deposited can be minimized or eliminated.

Detailed Description Text - DETX (4):

The present invention deposition process for **forming** the IMD layer can be carried out, after the heat treatment step, by flowing a precursor gas of silane, or precursor gases of silane and nitrous **oxide** into the plasma process chamber for the deposition process. The chamber pressure is normally kept at lower than 10.sup.-2 Torr. The process may be carried out at a chamber temperature of about 400.degree. C.

Detailed Description Text - DETX (5):

The present invention novel method for treating a dielectric film to suppress **high-density plasma** (HDP) oxide defect can be carried out before the deposition process of the dielectric film in the plasma process chamber. The **high-density plasma** CVD method, with its excellent gap filling capability, has largely replaced sub-atmospheric pressure CVD for depositing inter-metal-dielectric layers as the semiconductor fabrication process continuously shrinking to deep-sub-micron levels. The present invention novel

method minimizes or eliminates the as-deposited film cracking problem, particularly severe at the wafer edge, which may lead to device defects such as a short between interconnect metal lines.

Detailed Description Text - DETX (6):

The present invention novel **high-density plasma** (HDP) treatment method can be used to heat wafers to a temperature of up to 400.degree. C. to outgas the wafer surface in the HDP chamber prior to the deposition process, such that wafer edge void formation (or bubbling) and cracking can be eliminated. The fabrication yield of the HDP process can be improved by more than 10% when the present invention pre-treatment method is used, for instance, by eliminating shorts between the interconnect lines. The heat treatment process can be advantageously conducted at a temperature between about 300.degree. C. and about 400.degree. C.

DOCUMENT-IDENTIFIER: US 20020117256 A1

TITLE: Methods for fabricating flexible circuit structures

--------- KWIC ---------

Detail Description Paragraph - DETX (39):

[0076] The preferred magnetic source employed to achieve magnetically enhanced reactive ion etcher (RIE) used in practicing the present invention is a variable rotational field provided by the electromagnetic coils 142 and 143 arranged in a Helmholtz configuration. The electromagnetic coils 142 and 143 are driven by 3-phase AC currents. The magnetic field with Flux B is parallel to the structure 13 and perpendicular to the electrical field as shown in FIG. 28. Referring to FIG. 28 the vector of the magnetic field H which produces flux B is rotating around the center axis of the electrical field by varying the phases of current flowing through the electromagnetic coils 142 and 143 at a typical rotational frequency of 0.01 to 1 Hz, particularly at 0.5 Hz. The strength of the magnetic flux B typically varies from 0 Gauss to about 150 Gauss and is determined by quantities of the currents supplied to the electromagnetic coils 142 and 143. While FIG. 27 illustrates one **plasma** processing apparatus that is suitable for producing a **plasma for treating** the surface of the dielectric film 60, it is to be understood that other reactive ion producers may be employed, such as electron cyclotron resonance (**ECR**), helicon resonance or inductively coupled **plasma** (ICP), triode etchers, etc. Therefore, the source of the **plasma** may be any suitable source, such as electron cyclotron resonance (**ECR**), helicon resonance or inductively coupled **plasma** (ICP)-type sources. All three are in use on production equipment today. The main difference is that **ECR** and helicon sources employ an external magnetic field to shape and contain the plasma, while ICP sources do not.

US-PAT-NO: 6677251

DOCUMENT-IDENTIFIER: US 6677251 B1

TITLE: Method for forming a hydrophilic surface on low-k dielectric insulating layers for improved adhesion

---------- KWIC ---------

Detailed Description Text - DETX (6):

In the hydrophilicity increasing surface treatment method according to the present invention, in one embodiment, the method includes **treating** the surface of the dielectric insulating layer according to a dry **plasma** process. The plasma process for carrying out the plasma surface treatment may include any conventional plasma reactor configuration and plasma source including high density, medium density and low density plasmas. For example, for a high density plasma (HDP), the plasma source may include an electron-cyclotron-resonance (**ECR**) source, a helicon plasma source, an inductively coupled plasma (ICP) source, a dual plasma source (DPS) , or a magnetically enhanced RIE (MERIE). Preferably, the plasma reactor is a conventional PECVD or HDP-CVD reactor.

US-PAT-NO: 6572780

DOCUMENT-IDENTIFIER: US 6572780 B2

TITLE: Methods for fabricating flexible circuit structures

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Detailed Description Text - DETX (41):

The preferred magnetic source employed to achieve magnetically enhanced reactive ion etcher (RIE) used in practicing the present invention is a variable rotational field provided by the electromagnetic coils 142 and 143 arranged in a Helmholtz configuration. The electromagnetic coils 142 and 143 are driven by 3-phase AC currents. The magnetic field with Flux B is parallel to the structure 13 and perpendicular to the electrical field as shown in FIG. 28. Referring to FIG. 28 the vector of the magnetic field H which produces flux B is rotating around the center axis of the electrical field by varying the phases of current flowing through the electromagnetic coils 142 and 143 at a typical rotational frequency of 0.01 to 1 Hz, particularly at 0.5 Hz. The strength of the magnetic flux B typically varies from 0 Gauss to about 150 Gauss and is determined by quantities of the currents supplied to the electromagnetic coils 142 and 143. While FIG. 27 illustrates one **plasma** processing apparatus that is suitable for producing a **plasma for treating** the surface of the dielectric film 60, it is to be understood that other reactive ion producers may be employed, such as electron cyclotron resonance (**ECR**), helicon resonance or inductively coupled **plasma** (ICP), triode etchers, etc. Therefore, the source of the **plasma** may be any suitable source, such as electron cyclotron resonance (**ECR**), helicon resonance or inductively coupled **plasma** (ICP)-type sources. All three are in use on production equipment today. The main difference is that **ECR** and helicon sources employ an external magnetic field to shape and contain the plasma, while ICP sources do not.

US-PAT-NO: 6689646

DOCUMENT-IDENTIFIER: US 6689646 B1

TITLE: Plasma method for fabricating oxide thin films

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Detailed Description Text - DETX (7):
In some aspects, the oxide layer 402 and the sub-layer 506 are formed using a **transmission/transformer coupled plasma** (TCP) source (not shown). The use of a TCP source results in the same oxide layer 402 and sub-layer 506 bulk and interface characteristics as those associated with the use of an ICP source. However, the TCP source allows the process to be scaled up for larger applications, such as LCDs.

Detailed Description Text - DETX (22):
FIG. 10 is a flowchart illustrating the present invention method for fabricating a thin film oxide. The method starts with Step 1000. Step 1002 forms a first silicon layer. Step 1004 applies a second silicon layer overlying the first silicon layer. Step 1006 oxidizes the second silicon layer at a temperature of less than 400.degree. C. using a **transmission/transformer coupled plasma** source. Step 1008 forms a thin film oxide layer overlying the first silicon layer at a temperature of less than 400.degree. C. using a **transmission/transformer coupled plasma** source. Step 1010 plasma oxidizes the second silicon layer. In some aspects of the method, plasma oxidizing the second silicon layer in Step 1010 includes forming a thin film oxide layer more than 20 nm thick and forming the thin film oxide layer with a refractive index between approximately 1.45 and 1.47.

Claims Text - CLTX (21):
21. A method for fabricating a thin film oxide, the method comprising: forming a first silicon layer; applying a second silicon layer overlying the first silicon layer; oxidizing the second silicon layer at a temperature of loss than 400.degree. C. using a **transmission/transformer coupled plasma** source; and, forming an oxide layer overlying the first silicon layer at a temperature of less than 400.degree. C. using a **transmission/transformer coupled plasma** source.

Claims Text - CLTX (22):

22. The method of claim 21 wherein oxidizing the second silicon layer at a temperature of less than 400.degree. C. using a **transmission/transformer coupled plasma** source includes plasma oxidizing the second silicon layer.